



DOEACC CENTRE CALICUT  
COURSE PROSPECTUS

CDS/CA/7.5.1/F 40/R0

Name of the Group: VLSI Design Group

Name of the Course: Certificate Program in Embedded Hardware Modeling using Verilog HDL

Course Code: VL-555

Starting Dates: 15<sup>th</sup> February 2010 - **postponed to 9th April 2010**

Duration: 7 Days

Preamble: VLSI (Very Large Scale Integration) technology has emerged as a very important technology to provide tremendous quantum of processing power and functionality to modern electronic systems. Ubiquitous Computing and Embedded Systems, based on VLSI are revolutionizing every walks of our daily lives, be it Consumer Electronics, Communication, Computing, Automation, Space Application, Defense and to just about everything. With the advancements in silicon processing technologies for MEMS, NEMS and RF components, many of the formerly external components can now be integrated into a single System-on-Chip which has resulted in a dramatic improvements in performance while achieving reduction in the size, cost and power consumption. Complexity in such systems arises not only from the diversity of the technologies, from sensors and actuators and RF front-ends to base-band DSP software, etc., that must be integrated on-chip comprising of tens of millions of transistors, but also from the fact that such systems must be increasingly built from parts that have been designed separately and using different tools and flows.

Objective of the Course: The main objective of this course is to acquaint participants with Digital System & RTL design fundamentals and provide them with practical knowledge about the methodology and EDA tools used for these designs. This course may also help participants to implement relevant concepts for their research & academic projects.

Outcome of the Course: The participants will learn how to do RTL design of Hardware Building Blocks and perform verification using the powerful Verilog HDL.

Course Structure:

CDS/CA/7.5.1/F 40/R0

The VL555 is a 7 days, intensive hands-on training program.

Other Contents

- a. Course Fees : Course Fee is Rs.3000.00 plus service tax at actual
- b. Eligibility: Engineering (Degree or Diploma) OR Science Degree which includes a basic course in Digital Electronics. Students of such programs, who have taken a basic course in Digital Electronics may also apply
- c. Number of Seats : 30
- d. How to Apply :

Prospective participants are advised to apply in the prescribed Application Form available with the course brochure/course prospectus or downloaded from our website. Filled in application forms along with a Demand Draft towards advance fee of Rs.1000/- drawn in favour of **The Director, DOEACC Centre, Calicut, Payable at State Bank of India, CREC Branch, Chathamangalam** should be sent to the **Training Officer, DOEACC Centre Calicut, P. B. No. 5, NIT Campus Post, CALICUT – 673 601, Kerala. The Name of the Course Applied for should be super scribed on the top of the cover in which the application form is forwarded.**

You can also apply online at [www.doeaccalicut.ac.in](http://www.doeaccalicut.ac.in)

Hostel accommodation (if required) can be reserved on payment of Rs.500/- along with the advance fee.

- e. Selection of candidates: Candidates will be selected based on a first come first served basis subject to eligibility and availability of seats. All selected candidates shall be intimated of their selection by email and/or by letter.

**Mode of fee Payments** : *(Any 1 of the 3 options given below may be used to pay the fees)*

1. Demand Draft to be drawn in favor of Director, DOEACC Center Calicut, Payable at State Bank of India, Calicut NIT Branch(2207). The DD should reach here before the last date to apply.
2. Using the pay in slip available in our web site, through any branch of SBI (where this format is accepted). The **original counterfoil** should reach here before the last date to apply.
3. The fees can be paid by DD or can be paid directly into our account from any bank where core banking facility is available. The details required for direct payment are as given below.

**Current Account No:** : **010401158037**  
**Bank Name** : **SBI, NITC Chathamangalam**  
**Bank Code** : **2207**  
**IFC No** : **SBIN0002207**

The depositor should obtain the **UTR Number** from the branch while depositing cash directly into our account. Depositor should also obtain the acknowledgement duly filled up and signed by the staff of the bank through which the amount was deposited. UTR number should be mentioned in all the correspondences to us pertaining to amount. The following details are to be given by the depositor.

1. Name of the Depositor
2. Name of the Student
3. Date of Payment
4. Amount Deposited
5. Name of Bank/branch through which amount deposited
6. Purpose – Course ID – Advance Fee/Hostel Rent/Installment Fee etc.
7. Proof of Deposit (counterfoil/acknowledgement in **original**)
8. UTR Number

The Centre will not be responsible for any mistakes done by either the bank concerned or by the depositor while remitting the amount into our account

f. Test/Interview (if applicable) : NA

g. Counseling/Admission: 15th February 2010 -postponed to 9th April 2010

h. Admission Procedure :

Students who have been selected for test/interview/counseling/admission are required to report to the Centre on the prescribed day by 9:30 hrs along with the following

1. Attested Copies of Proof of Age, Qualifications, etc
2. Original Certificate of the above
3. Two copies of photograph and one stamp size photograph for identity card.
4. SC/ST Certificate (if applicable)
5. Income Certificate (if applicable)

The students on reaching the Centre are required to meet the Front Office Councilor (FOC). The FOC then directs the student to the Course Coordinator. The student gets the enrollment form verified by the Course Coordinator and then meets the FOC who shall direct the student to the Accounts for payment of fees. A student is thus admitted.

- i. Discontinuing the course: No fees under any circumstances shall be refunded in the event of a student discontinuing the course. A student can however, be eligible for module certificates (applicable only for courses with CDS/GA/7.5/15/40/80 regular admission) which he has successfully completed provided he has paid the entire course fees.
- j. Course Timings: 9.30 AM to 12.30 PM and 1.30 PM to 5.00 PM.

k. Location and How to reach :

DOEACC CENTRE Calicut is located very near to NIT (REC) campus and is about 22Kms from the Calicut (Kozhikode) city. A number of buses [Buses to NIT via Kunnamangalam] are available from "Palayam Bus Stand or KSRTC Bus Stand". Our stop is called "Panthrand" & is one stop before NIT. The bus fare is Rs.10/- from Calicut City to DOEACC Centre and is on the right side.

The Calicut (Kozhikode) is well connected by Rail, Road and Air from different parts of the country. The climatic conditions in Calicut are perhaps one of the best in India throughout the year. The maximum and minimum temperatures range between 35 and 20°C. The cool breeze further adds the comfort.

l. Course enquiries :

Students can enquire about the various courses either on telephone or by personal contact between 9.15 A.M. to 5.15 P.M. (Lunch time 1.00 pm to 1.30 pm).

m. Important Dates (if applicable) :

|   |             |
|---|-------------|
| Last date for receiving completed application forms | :09-04-2010 |
| Counseling/admission & Commencement of classes      | :09-04-2010 |
| Payment of fees                                     | :09-04-2010 |

Ph # (O) +91-495-2287266/67

Ph# (M) +919995427802 (Program Coordinator)

n. Placement : We have a placement cell, which provides placement assistance to students who qualify our courses

o. Hostel facilities :

Hostel accommodation is available for boys and girls on daily or monthly chargeable basis. The hostel fee varies from 450/- to 625/- per month depending on the location of accommodation. However, students are required to pay the hostel fees for the duration of the course for which they are seeking admission at the time of joining the course.

p. Canteen facilities :

The Centre has a canteen functioning at the main campus and food at reasonable rates is available for breakfast, lunch, and dinner

q. Lab Facilities

Altera Trainer kits, Xilinx Trainer Kits  
Xilinx ISE Design Suite,  
Altera Quartus II Design Suite,  
Complete range of Simulation, Synthesis Tools from Mentor Graphics  
FPGA Design and Verification Tools  
ASIC Design and Verification Tools  
Hardware-Software Co-verification Tools  
IC Nanometer Design Tools (Back end tools)  
System Modeling Tools, Universal Programmer,  
Digital Storage & Mixed Signal Oscilloscopes  
Cypress Semiconductor –DOEACC Joint PSoC LAB Resources  
SMD Reworkstation

r. Course Contents :

Introduction to Verilog HDL & EDA Tool(s)

Hierarchical Modeling Concepts.

Basic Concepts & Lexical Conventions.

Gate Level Modeling.

Structural Modeling.

Data Flow Modeling.

Behavioral Modeling.

Mini Project