



**NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT),  
CALICUT**

(Formerly DOEACC CENTRE CALICUT)

CDS/CA/7.5.1/F 40/R1

COURSE PROSPECTUS

Name of the Group: VLSI Design Group

Name of the Course: PG Diploma in ASIC Design and Verification

Course Code: VL 600

Starting Date: 22<sup>nd</sup> February 2012

Duration: 24 weeks

**Preamble:** The term ASIC stands for Application Specific Integrated Circuit. It is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use. Generally an ASIC design will be undertaken for a product that will have a large production run, and the ASIC may contain a very large part of the electronics needed on a single integrated circuit. As feature sizes are shrinking and design tools improved over the years, the complexity in an ASIC has grown to over 100 million gates. In ASIC Design and Verification process, Verification consumes 50% to 70% of the effort of design cycle and is on the critical path in the design flow of multimillion gate ASICs. Hence verification has become the main bottleneck in the design process. The functional verification bottleneck is an effect of raising the design abstraction level. Majority of ASICs require at least one re-spin, and 71% of re-spins are due to functional bugs. Since ASIC Verification is time consuming, adopting proper verification methodology in ASIC Design flow is extremely important. An ASIC Verification methodology provides the building blocks needed to quickly develop well-constructed and reusable verification components and test environments. FPGA Emulation is another means of verifying complex ASICs, and it helps to capture real time bugs.

b. Objective of the Course:

Education in Engineering Colleges and Universities are severely lagging in meeting VLSI Industry's specific needs, which creates a big gap between the Industry's requirements and the skills of the fresh engineering graduates. **Post Graduate Diploma in ASIC Design and Verification** is structured towards bridging this Industry-Academia gap by providing ASIC/VLSI Industry specific courses with focus on Advanced Technical and Personal Skill development.

The Course designed in consultation with the ASIC/VLSI industry experts with decades of experience working for various MNCs, builds on the basic concepts in ASIC Design and Verification, and then moves to Advanced ASIC development and Verification Techniques and Methodologies. The course transforms a raw engineering



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graduate into a capable ASIC Design and Verification professional with both technical and soft skills as required by the industry

Outcome of the Course: *This course is frequently updated in synchronization with the industry to provide the trainees in-depth knowledge and skills required by ASIC Design and Verification markets around the globe. It provides comprehensive understanding about the fundamental principles, methodologies and industry practices. This uniquely hybrid course makes the successful participants readily employable in multiple roles available in relevant industries. For people interested in entrepreneurship this would be an excellent launch pad. In addition the course also serves as a concrete platform for people involved in application research, consultancy and high end product development in both industry and academia.*

c. Course Structure:

*The VL600 contains seven modules. The students are required to do a project work in ASIC Design and Verification for a minimum period of 4 weeks to be eligible for issue of PG Diploma in ASIC Design and Verification.*

<b>VL 600</b>	<b>Module Name</b>	<b>Duration</b>
VL 601	Hardware Description Languages-Verilog	3 weeks
VL 602	Functional Verification	2 weeks
VL 603	Advanced Verification Language-System Verilog	4 weeks
VL 604	Assertion based Verification	2 weeks
VL 605	Coverage driven Verification and Functional Coverage in SV	2 weeks
VL 606	DPI and Verification Methodology	4 weeks
VL 607	ASIC Prototyping	3 weeks
VL 608	Project	4 weeks



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**Other Contents**

**a. Course Fees:**

**For SC/ST Category Applicants** : Total Fee payable is **Rs. 5650.00/\*-** (All inclusive, single payment. \* Conditions Apply).

**General Category Applicants:** Total Fee payable is **Rs.68000.00/ + Service Tax**  
*The course fee can be paid in maximum of three installments as given below*

**First Installment:** Rs. 30,000+Service Tax+ Admission Fee (Rs.250)

The students in the **first selection list** have to pay the first installment fee for taking provisional admission. (See **important dates** in page 7)

**Second Installment:** Rs. 25,000/+Service Tax

Second installment has to be paid on or before the date of counseling (22<sup>nd</sup> February 2012)

The students in the **additional selection list** have to pay both the first & second installment fee together on or before the date of counseling.

**Third Installment:** Rs. 13000/+Service Tax

Third installment has to be paid on or before 28<sup>th</sup> March 2012

- **Eligibility:** M.E/M.Tech/BE /B.Tech in Electronics/ Electronics & Communication/ Electrical/ Instrumentation/Computer Science/IT or M.Sc (Electronics). Diploma students may also be considered. Graduates with appropriate experience and final year students<sup>#</sup> also may apply  
<sup>#</sup> Final year students have to include the copies of course completion certificate of their qualifying degree/ diploma or copies of the mark lists up to the last semester/ year. On the date of counseling/ admission, he/she must produce the originals of course completion certificate/ mark lists up to the last semester/year examination

- **Number of Seats:** 40  
*SC/ST candidates and Persons with disabilities are eligible for seat reservation and relaxation in the minimum marks for eligibility.*
- **How to Apply :**

**Procedure for Online application:** Students can apply online by filling up the online application form. The students are first required to obtain the DD for



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Rs.1000/- (Rs.500 for SC/ST) towards advance deposit. The students are required to fill the details with regards to the DD Number, Date and Amount. The students are requested to note down their registration number allotted after pressing the "Submit" button and forward the demand draft mentioning their name, their online registration number and course code (i.e. VL600), on the back side of the DD. Online registrations not containing the processing fee details will not be considered for processing.

**Procedure for applying using the offline Application form:** The students can download the application form from our web site and fill the particulars and forward the same to the Training Officer along with the requisite fee as mentioned above.

Filled in application forms and Demand Draft should be sent to the **Training Officer, National Institute of Electronics and Information Technology, P. B. No. 5, NIT Campus Post, CALICUT – 673 601, Kerala.**

***The Name of the Course Applied for ( VL600: PG Diploma in ASIC Design & Verification) should be super scribed on the top of the cover in which the application form is forwarded.***

**b. Selection of candidates:**

*Candidates will be selected based on their marks in their qualifying examination subject to eligibility and availability of seats. Selection of candidates who have completed the course but expecting the results shall be based on the availability of seats. All selected candidates shall be intimated of their selection by **email alone**. The list of selected candidates shall be published in our website*

*The admission to the course shall be based on the following criteria:*

- 1. Should have passed the eligibility criteria as mentioned above.*

*Selection list of students will be prepared and published in our website as follows.*

***First selection list will be prepared based on the applications received on or before 24<sup>th</sup> January 2012.***

***The additional selection list will be prepared, if there are vacant seats, based on the applications received on or before 15<sup>th</sup> Feb 2012 and excluding the applicants included in the first selection list.***



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**Mode of fee Payments** : (Any 1 of the 3 options given below may be used to pay the fees)

1. Demand Draft to be drawn in favor of **Director, NIELIT Calicut** Payable at **State Bank of India, Calicut NIT Branch(2207)**. The DD should reach here before the last date mentioned.

2. Using the pay **in slip** available <http://www.doeacccalicut.ac.in/course/payinslip.pdf> **in our web site**, through any branch of SBI (where this format is accepted). The **original counterfoil** should reach here before the last date to mentioned, below.

3. The fees can be paid by DD or can be paid **directly into our account** from any bank where core banking facility is available. The details required for direct payment are as given below.

Name of Beneficiary	:	Director, NIELIT Calicut.
Savings Account No	:	31732177476
Bank Name	:	SBI, NITC Chathamangalam
Bank Code	:	2207
IFSC No	:	SBIN0002207

The depositor should obtain the **UTR Number** from the branch while depositing cash directly into our account. Depositor should also obtain the acknowledgment duly filled up and signed by the staff of the bank through which the amount was deposited. UTR number should be mentioned in all the correspondences to us pertaining to amount. The following details have to be communicated by the depositor, via email to: **trng@cedtic.com** AND copy to: **jayaraj@cedtic.com**



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1. Name of the Depositor
2. Name of the Student
3. Date of Payment
4. Amount Deposited
5. Name of Bank/branch through which amount deposited
6. Purpose –Course ID (VL600)–advance deposit/Hostel Rent/Installment Fee etc.
7. Proof of Deposit (copy of counterfoil/acknowledgment duly signed by the bank staff) .Original receipt should be retained, by the applicant, for producing on the date of counseling
8. Unique Transaction Reference (UTR) Number

*The Institute will not be responsible for any mistakes done by either the bank concerned or by the depositor while remitting the amount into our account*

- c. Test/Interview (if applicable) : N/A
- d. Counseling/Admission: 22<sup>nd</sup> February 2012.
- e. **Admission Procedure :**

Students who have been selected for counseling/admission are required to report to the Centre on the prescribed day by 9:30 hrs along with the following

1. Attested Copies of Proof of Age, Qualifications, etc
2. Original Certificate of the above
3. Two copies of passport size photographs and one stamp size photograph for identity card.
4. SC/ST Certificate in English/Hindi (if applicable)
5. Income Certificate in English/Hindi (if applicable)
6. Proof of Payment(s) made (counterfoil in original duly signed by the bank staff)

The students on reaching the Centre are required to meet the Front Office Councilor (FOC). The FOC then directs the student to the Course Coordinator. The student gets the enrollment form verified by the Course Coordinator and then meets the FOC who shall direct the student to the Accounts section for payment of fees. A student is thus admitted.



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- f. **Discontinuing the course:** *No fees under any circumstances shall be refunded in the event of a student discontinuing the course. A student can however, be eligible for module certificates (applicable only for courses which provide for modular admission) for modules he has successfully completed provided he has paid the entire course fees.*
- g. **Course Timings:** *The classes and labs are from 9.30 am to 12.30 pm and 1.30 pm to 5 pm Monday to Friday.*
- h. **Location and How to reach :**

*National Institute of Electronics and Information Technology is located very near to NIT (REC) campus and is about 22Kms from the Calicut (Kozhikode) city. A number of buses [Buses to NIT via Kunnamangalam] are available from "Palayam Bus Stand or KSRTC Bus Stand". Our stop is called "CEDT/Pandrandu" & is one stop before NIT. The bus fare is Rs.13/- from Calicut City to National Institute of Electronics and Information Technology and is on the right side.*

*Calicut (Kozhikode) is well connected by Rail, Road and Air from different parts of the country. The climatic conditions in Calicut are perhaps one of the best in India throughout the year. The maximum and minimum temperatures range between 35 and 20°C. The cool breeze further adds to the comfort.*

- i. **Course enquiries :**  
*Students can enquire about the various courses either on telephone or by personal contact between 9.15 A.M. to 5.15 P.M. (Lunch time 1.00 pm to 1.30 pm).*

Contact Details	
VL 600 Course Coordinator	9495642541/0495-2287266-222
Course Coordinator's email	jayaraj@cedtic.com
Training Officer	0495 – 2287266/ 2287268
Training Officer's E-mail:	trng@cedtic.com
Office Fax	0495 - 2287168



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**j. Important Dates:**

<i>Last date for receiving completed application forms</i>	<b>First selection list will be prepared based on the applications received on or before 24<sup>th</sup> Jan 2012.</b>  <b>The additional selection list will be prepared based on the applications received on or before 15<sup>th</sup> Feb 2012 and excluding the applicants, included in the first selection list.</b>
<i>Publication of <b>first selection list</b> in the Website <a href="http://www.cedtic.com">http://www.cedtic.com</a></i>	<b>25<sup>th</sup> Jan 2012.</b>
<i>Last date for taking provisional admission by paying the first installment of fees, for applicants in the first selection list</i>	<b>11<sup>th</sup> Feb 2012.</b>
<i>Publication of <b>additional selection list</b> in our website (if there are vacant seats)</i>	<b>15<sup>th</sup> Feb 2012</b>
<i>Counseling date</i>	<b>22<sup>th</sup> February 2012.</b>
<i>Class Commencement date</i>	<b>23<sup>st</sup> February 2012.</b>
<i>Payment of first installment of fees for applicants in <b>first selection list</b></i>	<b>11<sup>th</sup> Feb 2012.</b>
<i>Payment of second installment fees for applicants in <b>first selection list</b></i>	<b>On or before 20<sup>th</sup> February 2012.</b>
<i>Payment of third installment fees</i>	<b>On or before 30<sup>th</sup> March 2012</b>

k. **Placement:** We have a placement cell, which provides placement assistance to students who qualify our courses. Partial list of our past students, placed is given in the website

**l. Hostel facilities :**

*Hostel accommodation is available (if needed) for boys and girls on daily or monthly chargeable basis. The hostel fee varies from Rs.450/- to Rs.1150/- per month depending on the location of accommodation. However, students are required to pay the hostel fees for the duration of the course for which they are seeking admission at the time of joining the course.*



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**m. Canteen facilities :**

*The Centre has a canteen functioning at the main campus and food at reasonable rates is available for breakfast, lunch, and dinner*

**n. Lab Facilities**

*Altera & Xilinx Development Boards & Trainer Kits  
Xilinx ISE, Altera Quartus II, NIOS II Trainer Kits  
ASIC Design & Verification tools from Synopsys  
Complete range of Simulation, Synthesis Tools from Mentor Graphics  
FPGA Design and Verification Tools  
ASIC Design Verification Tools  
Hardware-Software Co-verification Tools  
IC Nanometer Design Tools (Back end tools)  
System Modeling Tools  
Digital Storage & Mixed Signal Oscilloscopes  
Logic Analyser & SMD Reworkstation*

**o. Course Contents :**

**Module-1: Hardware Description Languages - Verilog**

ASIC Design Concepts, ASIC Design Flow-Frontend and backend, EDA tools for Front-end and backend, Hardware Modeling Overview ,Verilog Language Concepts, Modules and Ports ,Introduction to Test benches Verilog Operators and Expressions, Data Flow and behavior Level Modeling ,Verilog Procedural Statements ,Controlled Operation Statements ,Verilog Tasks and Functions ,Advanced Language Concepts, Finite State Machines, RTL Coding guidelines, linting.



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**Module-2: Functional Verification**

Introduction to Functional Verification ,Verification Cycle ,Test bench structures and different types of TBs Verification Flow ,Basic Verification environment, Verification components, Verification Planning ,Introduction to bus functional model Verification Planning ,Verification Technologies ,Stimulus and response

Introduction to Unix commands, vim editor, Perl and Tcl, Basics of Perl scripting, Array Fundamentals, Hashes Basics, Control structures, Functions, File I/O, Regular expression, Test automation using script.

**Module-3: Advanced Verification Languages - System Verilog**

Introduction to functional verification languages, Introduction to System Verilog, System Verilog data types. System Verilog procedures, Interfaces and modports, System Verilog routines. Introduction to object oriented programming , Classes and Objects, Inheritance , Composition, Inheritance v/s composition, Virtual methods. Parameterized classes, Virtual interface, Using OOP for verification, System Verilog Verification Constructs

**Module- 4: Assertion based verification**

Introduction to assertion, Overview of properties and assertion, Basics of properties and sequences, Advanced properties and sequences, Assertions in design and formal verification, some guidelines in assertion writing

**Module-5: Coverage Driven Verification and functional coverage in SV**

Coverage Driven Verification, Coverage Metrics, Code Coverage, Introduction to functional coverage, Functional coverage constructs, Assertion Coverage, Coverage measurement, Coverage Analysis

**Module-6: DPI and Verification Methodology**

Basics of PLI of Verilog, Direct Programming Interface, Verification Methodology (VMM) , Verification components, OVM Overview.

**Module-7 ASIC Prototyping**



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ASIC Prototyping using FPGAs, Importance and advantages of FPGA prototyping in ASIC Verification and Validation, Challenges in ASIC Prototyping, Design partitioning of Multimillion Gate ASIC into FPGAs, Embedded Logic Analyzers-Xilinx Chip Scope and ALTERA Signal Tap. Debugging in FPGA validation environment.

**Project**

*Project development cycle, Project planning and management, Introduction to Project Configuration management, version control system-cvs, quality assurance.*

**The following texts do not form part of the prospectus:**

Signature of the Course Coordinator:

Signature of the Training Officer

Director

Approved/Not Approved

Guide lines:

1. All texts in Italics are to be entered by the course coordinator.
2. The Course Prospectus to be put to Director for approval through Training Officer before issue